



UNITED STATES PATENT AND TRADEMARK OFFICE

AT

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/747,802	12/29/2003	Alec W. Smidt	INTEL12	1858
6980	7590	02/24/2005	EXAMINER	
TROUTMAN SANDERS LLP BANK OF AMERICA PLAZA, SUITE 5200 600 PEACHTREE STREET, NE ATLANTA, GA 30308-2216			AUDUONG, GENE NGHIA	
			ART UNIT	PAPER NUMBER
			2827	

DATE MAILED: 02/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/747,802

Applicant(s)

SMIDT ET AL.

Examiner

Gene N. Auduong

Art Unit

2827

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-44 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-44 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152..

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. ____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____. |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date ____. | 6) <input type="checkbox"/> Other: ____. |

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claim 1-44 are rejected under 35 U.S.C. 102(b) as being anticipated by Atsumi et al. (U.S. Pat. No. 5,392,253).

Regarding claim 39, Atsumi et al. disclose a memory, comprising: a control circuit to provide a plurality of first signals, at least one signal of the plurality of first signals having a first voltage (figure 1, row decoder circuit 2 provides a plurality of first signals, at least one signal of the plurality of the first signals having a first voltage due to the selecting or non-selecting state); a source of a limited current connected to a first node (a source, figure 2, transistor 26, of a limited current connected to a first node between transistor 26 and transistor 27); a first semiconductor device having an input connected to a bias voltage, and being connected between the first node and a second node (figure 2, first semiconductor device, transistor 26, having an input connected to a bias voltage; figure 1, a bias voltage supplying to the decoder from the switching circuit 4); a plurality of second semiconductor devices, the plurality being in a series-connected configuration (figure 2, a series connection of transistors 27), one end of the plurality being connected to the second node, each second semiconductor device (transistor 27) of the plurality of second semiconductor devices having an input connected to a corresponding first signal of the plurality of first signals (figure 2, row selection signals); a driver (figure 2, CMOS

Art Unit: 2827

22 consisting transistors 23 and 24) having an input connected to first node (node between transistor 26 and transistor 27) and an output to provide the second signal, the second signal having a second voltage, the second voltage being greater than the first voltage; and a memory cell responsive to the second signal (figure 2, CMOS transistor 22 providing the second signal, which is the driving/selecting signal to select a row of memory cells by word line 12; col. 5, lines 4+).

Regarding claim 40, Atsumi et al. disclose the circuit of claim 39 wherein the source of a limited current is a semiconductor device which performs as a weak current source (the source providing by the transistor 26 which pull-up the selecting signal by the source supply SW2 in the event the input signals is low).

Regarding claims 41-42, Atsumi et al. disclose the circuit of claim 39 wherein the source of a limited current is connected to a predetermined voltage (predetermined voltage SW2), wherein the first semiconductor device is rated to withstand the predetermined voltage, and wherein at least one second semiconductor device of the plurality of second semiconductor devices is not rated to withstand the predetermined voltage (transistor 26 is rated to hold-up the supply voltage SW2, and transistor 27 is not rated to withstand the predetermined voltage SW2).

Regarding claims 43-44, Atsumi et al. disclose the circuit of claim 39 wherein the first semiconductor device is a metal oxide semiconductor transistor having a gate, a drain, and a source, the gate being the input connected to the predetermined voltage, the drain being connected to the first node, and the source being connected to the second node.

Art Unit: 2827

Claims 1-5, 6-11, 12-16, 17-22, 23-27, 28-33, 24-38 are claiming the similar limitation as previously discussed in claims 39-44. Therefore, they are analyzed as previously discussed with respect to claims 39-44.

Conclusion

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gene N. Auduong whose telephone number is (571) 272-1773. The examiner can normally be reached on 9-5-4, alternate second Monday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hoai Ho can be reached on (571) 272-1777. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

GA
February 10, 2005



Gene N Auduong
Primary Examiner
Art Unit 2827